IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
In re application of: Lawrence A. Clevenger	Filed: 11/21/2003 Examiner: Jack S. J. Chen
Serial No. 10/707,122	Group Art Unit: 2813
Title: Back End Interconnect With a Shaped Interface	Docket #: FIS920030220US1

DECLARATION UNDER 37 C.F.R. §1.132

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Chih-Chao_Yang, hereby declare that:

1. I have a Ph.D. degree in Material Science and Engineering from Carnegie Mellon University, PA, U.S.A.

2. I am experienced in the field of semiconductor processing and am very knowledgeable about Back-end-of-line (BEOL) metallization applications and related processes and about the state of knowledge of workers in the art. I authored over 13 technical papers related to this field, which were published in various international conferences in the past 3 years, see reference below for details.

3. Since 2000 I have been employed at IBM Microelectronics Division in the field of semiconductor processing.

4. I have read and understood the above-referenced patent application and its prosecution in the U.S. Patent and Trademark Office.

5. I have read and understood the Malhotra and Kozbicki references cited by the Examiner in the prosecution of the referenced patent application.

6. Neither the Malhotra nor the Kozbicki refereces suggests to one skilled in the art a method of forming an interconnect structure that includes a step of removing material from the lower interconnect in a generally cone-shaped structure. In particular, both of the cited references show slight material

removal from the lower interconnect leaving a lower aperture that has a planar or horizontal lower surface. Further, neither of the cited references shows or suggests to one skilled in the art that the lower aperture should be cone-shaped.

7. The contents of claim 6, together with the contents of paragraphs 47, 49, 52 and 53 of the text indicate to one skilled in the art that the cone-shape of the lower aperture is significant and that having the height of the cane in the range greater than the radius is critical to the invention and provides an unexpected beneficial result indicated in paragraph 37.

8. One skilled in the art would also understand from paragraph 55 of the text that the range of height (h) of the cone shape that is greater than $(3)^{1.5}$ times the radius is also critical to achieving the full benefit of the invention.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were wade with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon.

by: Chih-Chao Yang

Dated: 10/10/05

References:

* "A New Method of Cleaning Cu/Organic Low-K Interconnect," **Advanced Metallization Conference**, San Diego, CA, USA, October 29-30 (2002).

* "Evaluation of CVD TiN(Si) for Cu/SiLK™ Integration: Electrical and Reliability," **Advanced Metallization Conference**, Montreal, Canada, October 21-23 (2003).

* "A 90nm Dual Damascene Hybrid (Organic/Inorganic) Low-k – Copper BEOL Integration Scheme," **Advanced Metallization Conference**, Montreal, Canada, October 21-23 (2003).

* "Comprehensive Reliability Evaluation of a 90nm CMOS Technology with Cu/PECVD Low-K BEOL," **International Reliability Physics Symptom**, Phoenix, AZ, USA, April 25-29 (2004).

* "Measurements of effective thermal conductivity for advanced interconnect structures with various composite low-k dielectrics," **International Reliability Physics Symptom**, Phoenix, AZ, USA, April 25-29 (2004).

* "Chip-to-Package Interaction for a 90nm Cu/PECVD Low-k Technology," **International Interconnect Technology Conference**, San Francisco, CA, USA, June 7-9 (2004).

* "Reliability, Yield, and Performance of a 90 nm SOI/Cu/SiCOH Technology," **International Interconnect Technology Conference**, San Francisco, CA, USA, June 7-9 (2004).

* "90nm SiCOH Technology in 300mm Manufacturing," **Advanced Metallization Conference**, San Diego, CA, USA, October 19-21 (2004).

* "Electrical and Reliability Evaluation of Cu/Low-k Integration: Exploration of PVD Barrier/Seed and CVD SiC(N,H) Cap Depositions," **Advanced Metallization Conference**, San Diego, CA, USA, October 19-21 (2004).

* "90 nm SiCOH Technology in 300 mm Manufacturing," **Advanced Metallization Conference**, San Diego, CA, USA, October 19-21 (2004).

* "Extendibility of PVD Barrier/Seed for BEOL Cu Metallization," **International Interconnect Technology Conference**, San Francisco, CA, USA, June 6-8 (2005).

* "Stress Migration Reliability of Copper Interconnect Stacked Via Structures with Adjacent Copper Plates in Low k- Dielectrics," **VLSI Multilevel Interconnection Conference**, Fremont, CA, USA, October 3-6 (2005).

* "Use of wafer level voltage ramp in detecting potential Time Dependent Dielectric Breakdown (TDDB) problems in 90nm Cu/CVD low-k interconnects," **VLSI Multilevel Interconnection Conference**, Fremont, CA, USA, October 3-6 (2005).